ANNA UNIVERSITY, CHENNAI

NON- AUTONOMOUS COLLEGES

AFFILIATED TO ANNA UNIVERSITY

M.E. APPLIED ELECTRONICS

REGULATIONS 2025

PROGRAMME OUTCOMES (POs):

PO	Programme Outcomes
PO1	An ability to independently carry out research /investigation and development work to solve practical problems
PO2	An ability to write and present a substantial technical report/document.
PO3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

PROGRAMME SPECIFIC OUTCOMES(PSOs):

PSO	Programme Specific Outcomes
PSO1	Ability to design and implement innovative solutions to solve complex problems in Applied Electronics.
PSO2	Competence to independently undertake research projects involving simulation, measurement, and product development in Applied Electronics-related fields.

ANNA UNIVERSITY, CHENNAI

POST GRADUATE CURRICULUM (NON.AUTONOMOUS AFFILIATED INSTITUTIONS)

Programme: M.E., Applied Electronics **Regulations:** 2025

Abbreviations:

BS – Basic Science (Mathematics, Physics, Chemistry)
ES – Engineering Science (General (**G**), Programme Core (**PC**), Programme Elective (**PE**)
SD – Skill Development
SL – Self Learning
OE – Open Elective

L – Laboratory Course
T – Theory
LIT – Laboratory Integrated Theory
PW – Project Work
TCP – Total Contact Period(s)

Semester I

S. No.	Course Code	Course Title	Type	Periods per week			TCP	Credits	Category
				L	T	P			
1.	MA25C05	Advanced Mathematical Methods (ECE)	T	4	0	0	4	4	BS
2.	AP25101	Statistical Signal Processing and Modeling	T	3	1	0	4	4	ES (PC)
3.	AP25C01	Advanced Digital System Design	T	3	1	0	4	4	ES (PC)
4.	AP25C02	Analog Integrated Circuit Design	T	3	0	0	3	3	ES (PC)
5.	AP25C03	Digital CMOS VLSI Design	T	3	0	0	3	3	ES (PC)
6.	AP25C04	Analog IC Design Laboratory	L	0	0	4	4	2	ES (PC)
7.	AP25102	Technical Seminar	-	0	0	2	2	1	SD
						Total	**24**	**21**	

Semester II

S. No.	Course Code	Course Title	Type	Periods per week			TCP	Credits	Category
				L	T	P			
1.		Industrial Internet of Things	T	3	1	0	4	4	ES (PC)
2.		High Speed Circuit Design	T	3	1	0	4	4	ES (PC)
3.		Programme Elective I	T	3	0	0	3	3	ES (PE)
4.		Embedded System Design	LIT	3	0	2	5	4	ES (PC)
5.		Industry Oriented Course I	---	1	0	0	1	1	SD
6.		Industrial Training	-	-	--	-	---	1	SD
7.		Self-Learning Course	-	-	--	-	---	1	--
						Total	**17**	**18**	

Semester III

S. No.	Course Code	Course Title	Type	Periods per week			TCP	Credits	Category
				L	T	P			
1.		Programme Elective II	T	3	0	0	3	3	ES (PE)
2.		Programme Elective III	T	3	0	0	3	3	ES (PE)
3.		Programme Elective IV	T	3	0	0	3	3	ES (PE)
4.		Open Elective	T	3	0	0	3	3	OE
5.		Industry Oriented Course II	---	1	0	0	1	1	SD
6.		Project Work I	---	0	0	12	12	6	SD
						Total	**25**	**19**	

Semester IV

S. No.	Course Code	Course Title	Type	Periods per week			TCP	Credits	Category
				L	T	P			
1.		Project Work II	---	0	0	24	24	12	SD
						Total Credits	**24**	**12**	

Programme Elective Courses (PE)

S. No.	Course Code	Course Title	Periods per week			Total Contact Periods	Credits
			L	T	P		
1.		Digital Image and Video Processing	3	0	0	3	3
2.		DSP Architecture and Programming	3	0	0	3	3
3.		RF Integrated Circuit Design	3	0	0	4	3
4.		Electromagnetic Interference and Compatibility	3	0	0	3	3
5.		Advanced Microprocessors and Microcontrollers Architectures	3	0	0	3	3
6.		Advanced Computer Architecture Design	3	0	0	3	3
7.		Signal Integrity for High Speed Design	3	0	0	3	3
8.		VLSI Interconnects	3	0	0	3	3
9.		Semiconductor Memory Design	3	0	0	3	3
10.		Algorithms For VLSI Physical Design Automation	3	0	0	3	3
11.		Statistical Analysis and Optimization for VLSI	3	0	0	3	3
12.		System on Chip Design	3	0	0	3	3
13.		Hardware /Software Co Design	3	0	0	3	3
14.		MEMS and NEMS	3	0	0	3	3
15.		Cryptography and Hardware Security	3	0	0	3	3
16.		Neuromorphic Computing	3	0	0	3	3
17.		Artificial Intelligence for Hardware Design	3	0	0	3	3
18.		IP Core Design and Protection	3	0	0	3	3
19.		Spintronics and Quantum Computing	3	0	0	3	3
20.		Analog and Mixed Signal VLSI Design	3	0	0	3	3

Semester I

MA25C05	Advanced Mathematical Methods (ECE)	L	T	P	C
		3	1	0	4

Course Objectives:

This course aims to equip students with advanced mathematical and computational techniques focuses on developing problem-solving skills for designing efficient circuits, communication protocols, and embedded systems.

Calculus of Variations: Variation and its properties, Euler's equation, Functionals dependent on first and higher order derivatives, Functionals dependent on functions of several independent variables, Some applications, Direct methods, Ritz method.

Queueing Models: Markovian queues, Birth and death processes, Single and multiple server queueing models, Little's formula, Queues with finite waiting rooms, Queues with impatient customers: Balking and reneging. Finite source models, M/G/1 queue, Pollaczek Khinchin formula, M/D/1 and M/EK/1 as special cases, Series queues, Open Jackson networks.

Graph Theory: Introduction to paths, trees, Isomorphism, Matrix coloring and directed graphs, Some basic algorithms: Dijkstra's Algorithm, Depth-First search, Breadth-First search, Prims Algorithm, Kruskal Algorithm

Optimization Techniques: Linear programming, Basic concepts, Graphical and simplex methods, Big M method, Transportation problems, Assignment problems.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. Elsgolc, L. D. – *Calculus of Variations*, Dover Publications.
2. Gross, D. & Harris, C. M. – *Fundamentals of Queueing Theory*, Wiley.
3. Deo, N.–*Graph Theory with Applications to Engineering and Computer Science*, PHI.
4. Hillier, F. S. & Lieberman, G. J –*Introduction to Operations Research*, McGraw-Hill.
5. Kanti Swarup, Gupta P.K.,& Man Mohan–*OperationsResearch*, Sultan Chand &Sons.

E-resources:

1. https://nptel.ac.in/courses/111/105/111105039
2. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-262-discrete-stochastic-processes
3. https://nptel.ac.in/courses/106/106/106106183

AP25101	Statistical Signal Processing and Modeling	L	T	P	C
		3	1	0	4

Course Objectives:

To introduce random signal processing, modeling for prediction and estimation, spectral estimation (parametric & non-parametric), and MSE/adaptive filter design.

Introduction to Random Signal Processing: Discrete random processes, ensemble averages, stationarity, bias & estimation, autocovariance, autocorrelation, Parseval's theorem, Wiener-Khintchine relation, white noise, PSD, spectral factorization, filtering.

Activites: 1.Simulate discrete random processes in MATLAB/Python.
2. Compute ensemble averages, autocorrelation & PSD for sample signals

Signal Modeling: AR, MA, ARMA models, forward/backward linear prediction, Yule-Walker method, Prony's equations, Levinson-Durbin algorithm.

Activites: 1. Implement AR, MA, ARMA models using time-series data
2. Perform forward and backward prediction

Spectral Estimation: Spectral estimation from finite signals, nonparametric methods (periodogram, Bartlett, Welch, Blackman-Tukey), parametric methods, AR spectral estimation, harmonic detection.

Activites: 1. Apply periodogram, Bartlett, and Blackman-Tukey methods on signals
2. Detect harmonic components using AR spectral estimation

Linear Estimation: LMMSE filtering, Wiener-Hopf equations, FIR/IIR Wiener filters, causal/non-causal filters, noise cancellation.

Activites: 1. Design FIR and IIR Wiener filters in MATLAB/Python
2. Solve Wiener-Hopf equations for given signals

Adaptive Filters: FIR adaptive filters, steepest descent, LMS, normalized LMS, RLS algorithm, adaptive equalization, echo & noise cancellation.

Activites: 1. Implement LMS, Normalized LMS, and RLS algorithms
2. Compare convergence behavior of adaptive algorithms

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. Hayes, M. H. (2002). Statistical digital signal processing and modeling. John Wiley & Sons, Inc.
2. Manolakis, D. G., & Ingle, V. K. (2011). Applied digital signal processing. Cambridge University Press.
3. Kay, S. M. (2017). Fundamentals of statistical signal processing: Estimation theory (Vol. 1),(vol 3) Detection theory (Vol. 2). Prentice Hall.
4. Kailath, T., Sayed, A. H., & Hassibi, B. (2000). Linear estimation. Prentice Hall.

	CO description	PO Mapping	PSO1	PSO2
CO1	Explain the concepts of random processes and their statistical properties.	-	-	-
CO2	Analyze signals using ARMA, AR, and MA models for prediction and analysis.	PO1(3) PO2(3)	3	3
CO3	Apply spectral estimation techniques to analyze signals in the frequency domain.	PO1(3) PO2(3)	2	2
CO4	Design and implement linear and adaptive filters for noise cancellation and signal enhancement.	PO1(3) PO3(3)	3	2

AP25C01	Advanced Digital System Design	L	T	P	C
		3	1	0	4

Course Objectives:

To study design and analysis of synchronous/asynchronous sequential circuits, PLD/ROM design, combinational/PLA testing, and Verilog HDL for digital system design.

Sequential Circuit Design: State diagrams/tables, state assignment & reduction, synchronous circuit design, iterative circuits, ASM charts.

Activities: 1. Design state diagrams for given problems
2. Implement synchronous circuits using ASM

Asynchronous Sequential Circuit Design: Flow table reduction, race conditions, hazards (static/dynamic/essential), mixed-mode circuits, vending machine controller design.

Activities: 1. Analyze and minimize flow tables
2.Identify and eliminate hazards

Fault Diagnosis and Testability Algorithms: Fault table, path sensitization, Boolean difference, D & Kohavi algorithms, PLA faults, DFT, BIST techniques.

Activities:1.Generate fault tables for combinational circuits
2. Simulate fault detection using D-algorithm

Synchronous Design Using Programmable Devices: PLD families, PLA/PAL-based circuit design, ROM design, FSM realization using PLDs, FPGA (Xilinx Vertex 7).

Activities:1. Iimplement FSM using PLA/PAL
2. Program and simulate FSM on FPGA

System Design Using Verilog: Verilog HDL modeling, data types, behavioral & structural modeling, FSM synthesis, test benches, combinational/sequential circuit realization.

Activities: 1. Write and simulate Verilog code for registers, counters, serial adders
2.Design and test a simple microprocessor in Verilog

Weightage: Continuous Assessment: 50%, End Semester Examinations: 50%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. Roth, C. H., Jr. (2013). Fundamentals of logic design (7th ed.). Thomson Learning.
2. Arnold, M. G. (1999). Verilog digital – computer design. Prentice Hall PTR.
3. Biswas, N. N. (2001). Logic design theory. Prentice Hall of India.
4. Lala, P. K. (2020). Fault tolerant and fault testable hardware design. B S Publications.
5. Lala, P. K. (2015). Digital system design using PLD (Reprint ed.). B S Publications.
6. Palnitkar, S. (2003). Verilog HDL – A guide to digital design and synthesis. Pearson.

	CO description	PO	PSO1	PSO2
CO1	Explain the fundamentals of synchronous and asynchronous sequential circuits	**-**	**-**	**-**
CO2	Analyze and design sequential circuits using state diagrams and ASM charts.	PO1(3)	2	2
CO3	Apply fault diagnosis and testability algorithms to digital circuits.	PO1(3) PO2(3)	3	3
CO4	Develop and simulate digital systems using Verilog HDL and FPGA.	PO1(3) PO2(3)	2	2

AP25C02	Analog Integrated Circuit Design	L	T	P	C
		3	0	0	3

Course Objectives:
To Study single-stage amplifier design, high-frequency/noise characteristics, operational amplifiers, voltage/current reference circuits with practical exercises

Single Stage Amplifiers: MOS physics, equivalent circuits, CS, CG, source follower, differential & cascode amplifiers, design for SR, gain, BW, ICMR, power, voltage swing.
Activities:1. Design and simulate CS, CG amplifiers
2. Calculate gain, bandwidth, slew rate for given specification

High Frequency and Noise Characteristics of Amplifiers: Miller effect, pole analysis, frequency response of stages, noise sources, noise analysis in single stage and differential amplifiers.
Activities:1. Analyze frequency response using pole-zero plots
2. Simulate noise performance in amplifiers.

Negative Feedback Amplifiers and Operational Amplifiers: Feedback types, loading effects, op-amp parameters, one/two-stage op-amps, gain boosting, slew rate, PSRR, noise in op-amps.
Activities: 1**.**Design and simulate negative feedback circuits
2. Evaluate gain, slew rate, and PSRR of op-amps

Stability and Frequency Compensation of Two Stage Operational Amplifier: Two-stage op-amp analysis, phase margin, compensation methods, slew rate issues, advanced compensation techniques.

Activities:1. Analyze phase margin and stability in two-stage op-amps
2. Implement frequency compensation methods in simulations

Voltage and Current References: Current mirrors (Wilson, Widlar, Cascode), high swing cascode sinks, supply/temperature independent biasing, PTAT & CTAT currents, constant-Gm biasing.

Activities: 1. Design and simulate various current mirrors
2. Implement PTAT and CTAT current references

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. Razavi, B. (2016). Design of analog CMOS integrated circuits (2nd ed.). Tata McGraw Hill.
2. Sansen, W. M. C. (2007). Analog design essentials. Springer.
3. Grebene, A. B. (2003). Bipolar and MOS analog integrated circuit design. John Wiley & Sons, Inc.
4. Allen, P. E., & Holberg, D. R. (2013). CMOS analog circuit design (3rd ed.). Oxford University Press.
5. Natarajan, A. (n.d.). EE5390: Analog IC Design [Recorded lecture]. Retrieved from http://www.ee.iitm.ac.in/~ani/ee5390/index.html
6. Baker, R. J. (2019). CMOS: Circuit design, layout, and simulation (4th ed.). Wiley IEEE Press.

	CO description	PO Mapping	PSO1	PSO2
CO1	Explain the theory and design concepts of analog circuits .	-	-	-
CO2	Analyse and design single-stage and multi-stage amplifiers considering high-frequency and noise characteristics to meet specified performance criteria.	PO1(3)	2	2
CO3	Apply concepts of negative feedback, stability, and frequency compensation in the design and analysis of operational amplifiers.	PO1(3) PO2(3)	3	3
CO4	Design and simulate voltage and current reference circuits with temperature and supply independence for analog integrated systems.	PO1(3) PO2(3)	2	2

AP25C03	Digital CMOS VLSI Design	L	T	P	C
		3	0	0	3

Course Objectives:

To Understand CMOS basics and design combinational/sequential circuits; apply structured VLSI design through case studies.

MOS Transistors and CMOS Inverter: MOS transistor characteristics, short channel effects, CMOS inverter design, stick diagrams, power, delay, sizing.
Activities:1. Simulate CMOS inverter characteristics and sizing effects
2. Draw stick diagrams and analyze power-delay trade

CMOS, Combinational Circuits: Complementary CMOS, power reduction, ratioed logic, pass transistor logic, dynamic CMOS, Domino, NP-CMOS.
Activities:1. Design combinational logic using different CMOS styles
2. Analyze power and switching activity in logic gates

CMOS, Sequential Circuits: Latches vs registers, flip-flops, dynamic/static registers, clocking strategies, Schmitt trigger, mono/astable circuits.

Activities:1. Implement various flip-flops and compare timing behavior
2. Design clocking schemes for latch/register pipelines

CMOS Sub System Design Adders (carry bypass, select, CLA), multipliers, counters, parity generators, multiplexers, shifters, memory elements.

Activities:1. Design fast adders and multipliers
2. Build and simulate small subsystems (e.g., counter + MUX)

Performance Estimation & Design Techniques:Delay estimation, logical effort, sizing, power, interconnects, scaling, synchronous and self-timed design.

Activities:1. Estimate delay and power for sample circuits
2. Compare synchronous vs self-timed circuit design .

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References

1. Weste, N. H. E., & Harris, D. (2011). *CMOS VLSI design:* A circuits and systems perspective. Pearson.
2. Rabaey, J. M., & Nikolić, B. (2003). Digital integrated circuits*. Pearson*.
3. Martin, K. (2011). Digital integrated circuit design. Oxford University Press.
4. Palnitkar, S. (2003). *Verilog HDL* (2nd ed.). Pearson Education.
5. Rabaey, J. M., Chandrakasan, A., & Nikolić, B. (2003). Digital integrated circuits . Pearson.

	CO description	PO	PSO1	PSO2
CO1	Explain CMOS basics in digital circuits.	-	-	-
CO2	Analyze and design CMOS-based combinational and sequential circuits	PO1(3)	2	2
CO3	Apply various CMOS logic styles and techniques to optimize digital subsystems	PO1(3) PO2(3)	3	3
CO4	Evaluate and estimate circuit performance using structured approaches for subsystem design.	PO1(3) PO2(3)	2	2

AP25C04	Analog IC Design Laboratory	L	T	P	C
		0	0	4	2

Course Objectives:

To Design analog circuits from transistor level to IA implementation using CAD tools for simulation, layout, LVS, and parasitic extraction.

List of Experiments

1. Extraction of process parameters of CMOS process transistors
   a. Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
   b. Plot ID vs. VGS at particular drain voltage for NMOS, PMOS and determine Vt.
   c. Plot log ID vs. VGS at particular gate voltage for NMOS, PMOS and determine IOFF and sub- threshold slope.
   d. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e. Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS of appropriate voltage To extract Vth use the following procedure.
      i. Plot gm vs VGS using SPICE and obtain peak gm point.
      ii. Plot y=ID/(gm) as a function of VGS using SPICE.
      iii. Use SPICE to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
   f. Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it.
2. CMOS inverter design and performance analysis
   a. i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
      ii. Plot VTC for CMOS inverter with varying VDD.
      iii. Plot VTC for CMOS inverter with varying device ratio.
   b. Perform transient analysis of CMOS inverter with no load and with load and determine propagation delay tpHL, tpLH, 20%-to-80% rise time tr and 80%-to-20% fall time tf.
   c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.
3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.
4. Single stage amplifier design and performance analysis
   a. Plot small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors.
   b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
      i. Establish a test bench to achieve VDSQ=VDD/2.
      ii. Calculate input bias voltage for a given bias current.

iii. Use spice and obtain the bias current. Compare with the theoretical value
iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier
v. using small signal analysis in spice, considering load capacitance.
vi. Plot step response of the amplifier with a specific input pulse amplitude.
vii. Derive time constant of the output and compare it with the time constant
viii. resulted from -3dB Band Width.
ix. Use spice to determine input voltage range of the amplifier

5. Three OPAMP Instrumentation Amplifier (INA).
Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
i. Draw the schematic of op-amp macro model.
ii. Draw the schematic of INA.
iii. Obtain parameters of the op-amp macro model such that it meets a given specification for: i.low-frequency voltage gain, ii. unity gain BW (fu), iii.input capacitance, iv.output resistance, v.CMRR
a. Draw schematic diagram of CMRR simulation setup.
b. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
c. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
d. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.

6.Use Layout editor.
a. Draw layout of a minimum size inverter using transistors from CMOS process library. Use Metal 1 as interconnect line between inverters.
b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.
c. Extract the netlist. Use extracted netlist and obtain tPHLtPLH for the inverter using Spice.
d. Use a specific interconnect length and connect and connect three inverters in a chain.
e. Extract the new netlist and obtain tPHL and tPLH of the middle inverter.
f. Compare new values of delay times with corresponding values obtained in part ‘c’.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter
a. low-frequency voltage gain,
b. unity gain BW (fu),
c. Power dissipation
i. Perform DC analysis and determine input common mode range and compare with the theoretical values.
ii. Perform time domain simulation and verify low frequency gain.
iii. Perform AC analysis and verify.

Weightage: Continuous Assessment: 60%, End Semester Examinations: 40%
Assessment Methodology: Project (30%), Assignment (10%), Practical (30%), Internal Examinations (30%)

	CO description	PO	PSO1	PSO2
CO1	Characterize MOS transistors and design basic analog building blocks using simulation tools.	PO1(3)	2	2
CO2	Implement and simulate analog circuits through schematic entry, layout design, LVS, and parasitic extraction.	PO1(3) PO2(3)	3	3
CO3	Design and validate an instrumentation amplifier using a structured analog design flow with CAD tools.	PO1(3) PO2(3)	2	2